WHAT IS CLAIMED IS:

1. A data processing device in which a processor processes data based on a stored program and a buffer manager accesses the data, comprising:

a program memory storing program codes, the program codes being loaded into the program memory and executed by the processor when processing the data;

a shared memory storing one of the program codes and the data; and

a control unit selectively connecting one of the processor and the buffer manager to the shared memory based on a select pattern, wherein the shared memory functions to store the program codes when the select pattern is set in a first condition, and the shared memory functions to store the data when the select pattern is set in a second condition.

2. The data processing device according to claim 1, wherein the control unit comprises a register and a multiplexer, the select pattern being input to the register, and the multiplexer selectively connecting one of a first connecting line and a second connecting line to the shared memory in response to the select pattern input to the register.

3. The data processing device according to claim 1, wherein, when the stored program includes a large amount of program codes exceeding a storage capacity of the program memory, both the program memory and the shared memory

function to store the program codes and an externally attached buffer memory is used to store the data, and when the stored program includes a small amount of program codes, only the program memory functions to store the program codes and the shared memory functions to store the data.

4. A signal processing device in which an internal logic circuit performs a logic operation for input signals, received from input terminals, and outputs processed signals to output terminals, comprising:

a register storing a pattern of addresses provided for selection of a signal being tested;

a selecting unit receiving respective testing signals of the internal logic circuit, and selecting a number of testing signals from among the received testing signals based on the pattern of addresses stored in the register; and

an output unit sequentially selecting one of the testing signals selected by the selecting unit, and outputting each selected testing signal to a test output terminal.

5. The signal processing device according to claim 4, further comprising a register setting unit provided between the input terminals and the test register, the register setting unit sending the pattern of addresses to the register so that the pattern of addresses is stored into the register.

6. The signal processing device according to claim 4, wherein the selecting unit comprises:

a decoder generating a select signal based on the pattern of addresses stored by the register; and

a selector receiving the respective testing signals from the internal logic circuit and selecting a number of testing signals from among the received testing signals in response to the select signal from the decoder.

7. The signal processing device according to claim 4, wherein the output unit comprises:

a sync circuit synchronizing the selected testing signals from the selecting unit with a clock signal; and

a multiplexer sequentially selecting one of the testing signals from the sync circuit based on the clock signal, and outputting each selected testing signal to the test output terminal.

8. The signal processing device according to claim 4, wherein the output unit includes a clock signal outputting unit which outputs a clock signal to a strobe terminal, the clock signal being generated from a reference clock signal of the internal logic circuit based a frequency-multiply factor from the register.

9. An interface device which performs data input/output operations through a plurality of channels, comprising:

a plurality of buffer memories including a first memory buffer and a second memory buffer, each buffer memory provided for a particular one of the plurality of channels; and

a control unit controlling the data input/output operations for each of the plurality of buffer memories such that data stored in the first buffer memory and data stored in the second buffer memory are set to be identical to each other by performing data transfer between the first buffer memory and the second buffer memory.

10. The interface device according to claim 9, wherein the control unit comprises a data management table which provides correlations between locations of respective data stored in the plurality of buffer memories and locations of data stored in a recording medium, respective states of the stored data in the plurality of buffer memories being managed by the control unit.

11. The interface device according to claim 10, wherein, when the stored data of one of the buffer memories is updated through one of the channels, the control unit sets the state of another channel in an access-disable state by using the data management table, thereby inhibiting receiving of a command at the interface device via said another channel.

12. The interface device according to claim 10, wherein, when a first data of the first buffer memory for one of the channels is renewed to a second data, the control unit transfers the second data of the first buffer memory to the second buffer memory for another channel through a data buffer during a time the interface device is in an idle state.

13. The interface device according to claim 12, wherein, when the data transferring is performed to the second buffer memory for said another channel, the control unit sets the state of said another channel in an access-disable state by using the data management table, thereby inhibiting receiving of a command at the interface device with respect to said another channel.